ABSTRACT

The invention describes the fabrication and structure of an ESD protection device for integrated circuit semiconductor devices with improved ESD protection and resiliency. A vertical bipolar npn transistor forms the basis of the protection device. To handle the large current requirements of an ESD incident, the bipolar transistor has multiple base and emitter elements formed in an npn bipolar array. To assure turn-on of the multiple elements of the array the emitter fingers are continuously or contiguously connected with an unique emitter design layout. The contiguous emitter design provides an improved electrical emitter connection for the device, minimizing any unbalance that can potentially occur when using separate emitter fingers and improving the ability for the simultaneous turn on of the multiple emitter-base elements. The emitter is contained within the footprint of the collector elements, and enables containment of device size, therefore minimizing device capacitance characteristics important in high speed circuit design. Other embodiments of the invention use variations in the structure of the common contiguous emitter conductor as well as different base conductor structure layouts.